

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

(12) UK Patent Application (19) GB (11) 2 204 456 A⁽¹³⁾

(43) Application published 9 Nov 1988

(21) Application No 8810391

(22) Date of filing 3 May 1988

(30) Priority data

(31) 874241

(32) 30 Apr 1987

(33) KR

(71) Applicant

Samsung Semiconductor & Telecommunications Co Ltd

(Incorporated in South Korea)

259 Gongdan-Dong, Gumi-City, Kyongsangbuk-Do, Republic of South Korea

(72) Inventors

Su-In Cho

Dong-Sun Min

(74) Agent and/or Address for Service

Appleyard Lees

15 Clare Road, Halifax HX1 2HY

(51) INT CL⁴

G05F 3/20 H02M 3/07

(52) Domestic classification (Edition J):

H2F CP

U1S 2121 H2F

(56) Documents cited

US 4439692

US 4438346

(58) Field of search

H2F

G3U

H2H

H3T

Selected US specifications from IPC sub-classes

G05F H02M H03K

(54) Substrate or back bias generator

(57) A circuit for generating a back bias voltage V_{BB} for use in a semiconductor memory device is disclosed, wherein the back bias voltage V_{BB} is clamped between desired voltage levels. The circuit comprises an oscillator 10 for generating a square wave having a specified frequency, a buffer 20 connected to buffer the output of the oscillator 10 to provide a square wave having a level of a source supply voltage V_{CC} , a charge pump circuit 30 for providing the back bias voltage V_{BB} by receiving the output of the buffer 20, and a clamping circuit 40 connected between the output of the charge pump circuit 30 and ground level V_{SS} for clamping within a specified range the back bias voltage V_{BB} provided by the charge pump circuit 30, to mitigate the effect of variations of the source supply voltage V_{CC} .

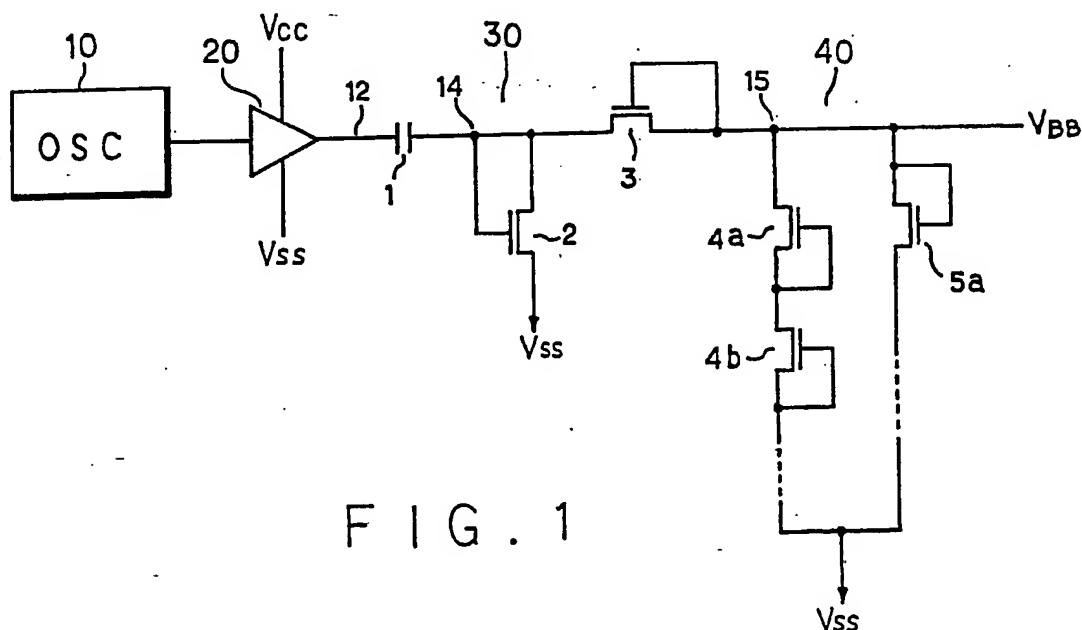


FIG. 1

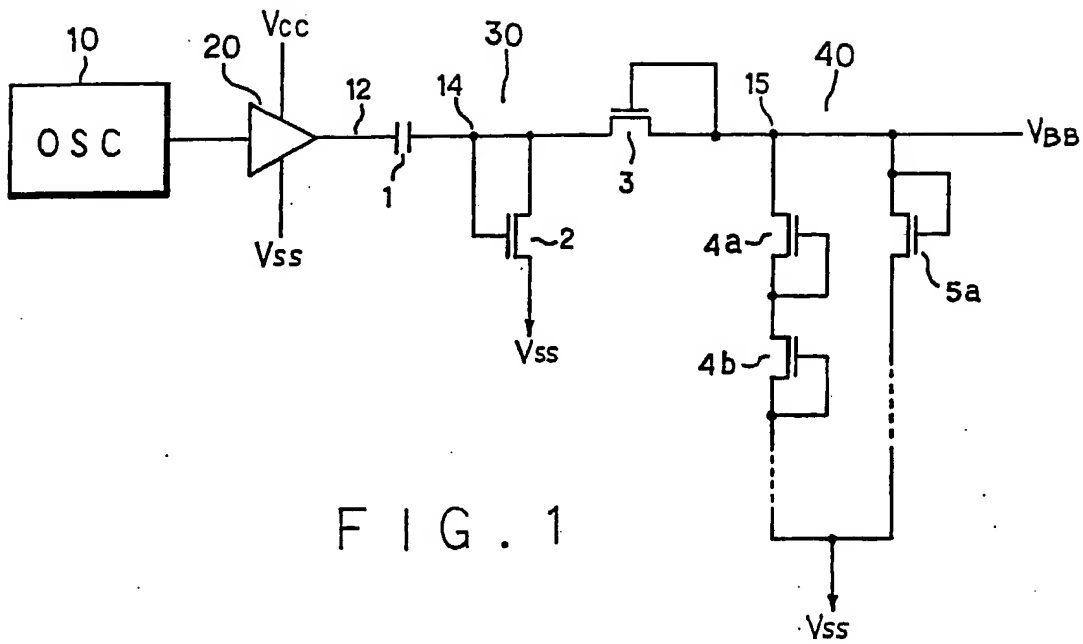


FIG. 1

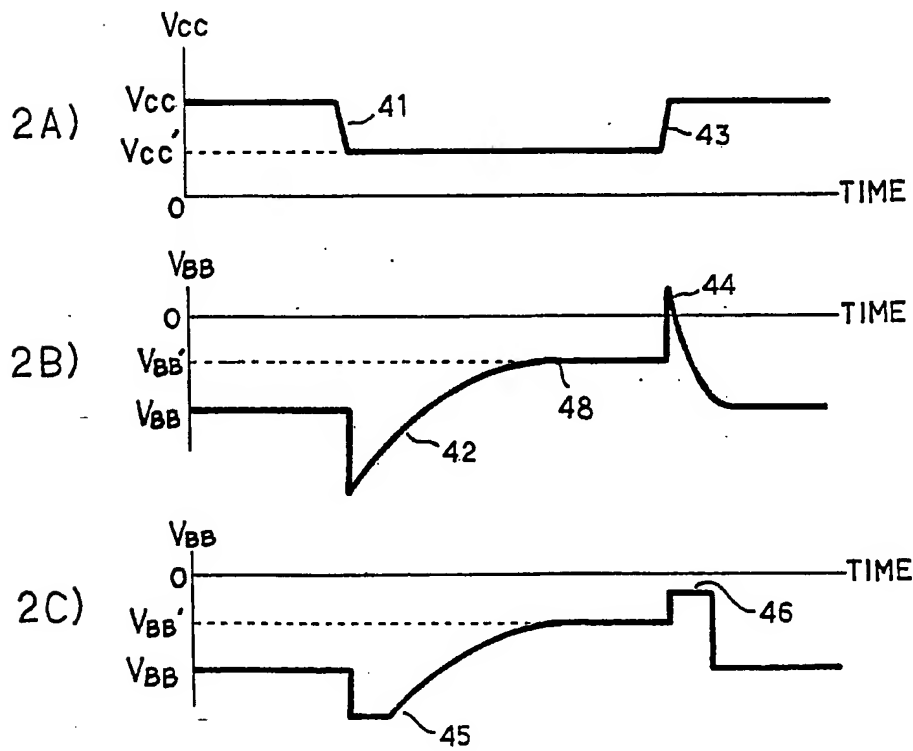


FIG. 2

BACK BIAS GENERATOR

This invention relates to semiconductor devices, and is concerned particularly although not exclusively with circuits for generating a back bias voltage in a semiconductor memory device.

A recently proposed semiconductor memory device has been equipped with an on-chip back bias generator in order to improve its performance and reduce the number of its external pins. The performance of a semiconductor memory device, formed in a P-type semiconductor substrate, can be improved by the application of a negative voltage (usually less than -2 volts) to the semiconductor substrate, whereby the threshold voltage of an N-channel MOS transistor formed in the substrate can be stabilized, and not only an increase in operating speed but also a reduction of leakage current can be achieved, due to a decrease of junction capacitance.

However, such an improvement of performance will be secured only where the back bias voltage is controlled to be within desired limits, during variations of power supply voltage. As a matter of fact, the power supply voltage delivered from an exterior power supply circuit to the semiconductor memory device may vary instantaneously, due to instabilities in the operation thereof and the introduction of noise. As a result of such variation of power supply voltage, the back bias generator may have a vital influence on the semiconductor memory device. That is, if the back bias voltage should fall by a large amount due to variation of the power supply voltage, the reverse bias voltage at N+/P junction regions in the substrate will increase and this may readily cause reverse breakdown. Also, if the back bias

voltage should rise above ground level, the N+/P junction regions will be forwardly biased and, as a result, the semiconductor memory device may be caused to malfunction as a whole.

5

It is an object of the invention to provide an improved back bias generator which enables the back bias voltage to be clamped within desired limits.

10 According to one aspect of the invention, there is provided a semiconductor device including a back bias generator for generating and supplying a back bias voltage to the semiconductor substrate, the generator comprising:

15

a oscillator for generating a square wave of a predetermined frequency;

20 a buffer connected to receive the square wave output of the oscillator and produce therefrom a similar square wave which alternates between a supply voltage level and another voltage level;

25 a charge pump circuit connected to receive the square wave output of the buffer and produce therefrom a back bias voltage to be applied to the semiconductor substrate; and

30 a clamping circuit which is connected between the output of the charge pump circuit and a ground level and is operative to clamp the level of the back bias voltage so that excursions thereof lie within a predetermined range.

35 Thus, the effect of variations in the supply

voltage upon the level of the back bias voltage may be reduced.

Preferably, the clamping circuit comprises a
5 first set of series connected semiconductor elements
arranged to conduct current only in one direction between
the output of the pump circuit and said ground level, and
a second set of series connected semiconductor elements
arranged to conduct current only in an opposite direction
10 between the output of the pump circuit and said ground
level, said first and second sets being connected in
parallel.

Each semiconductor element preferably comprises
15 an MOS transistor having a gate electrode connected to a
source or drain electrode thereof.

The invention may be applied with advantage to a
semiconductor memory device.

20

For a better understanding of the invention and
to show how the same may be carried into effect,
reference will now be made, by way of example, to the
accompanying drawing, in which:

25

Figure 1 is a schematic circuit diagram of a back
bias voltage generator for use in a semiconductor memory
device embodying the invention; and

30

Figure 2A is a waveform diagram showing
variations in supply voltage V_{cc} ;

Figure 2B is a waveform diagram showing a
theoretical output voltage without clamping; and

35

Figure 2C is a waveform diagram similar to Figure 2B, but showing the effects of a clamping circuit.

The back bias voltage generator shown in Figure 1 includes an oscillator 10, comprising a ring oscillator consisting of conventional inverters or a Schmitt trigger circuit with gates, for generating a square wave; a buffer circuit 20 for buffering the square wave output of the oscillator 10 into a square wave which alternates between a source supply voltage V_{CC} and a ground voltage V_{SS} ; a charge pump circuit 30 having a capacitor 1 and MOS transistors 2 and 3 for receiving the output of the buffer circuit 20 and providing a back bias voltage; and a clamping circuit 40 having MOS transistors (4a, 4b, and 5a...) for receiving the output of the charge pump circuit 30 and clamping out over-range and under-range portions of variations of the back bias voltage V_{BB} due to variations of the source supply voltage V_{CC} .

The frequency of the square wave output of the oscillator 10 is typically in the range 3 to 12 MHz and the duty cycle thereof is typically "1". The charge pump circuit 30 comprises a MOS capacitor 1 having a large capacitance, one electrode of which is connected to an output of the buffer circuit 20 and other electrode of which is connected to a node 14. To the node 14 are connected the drain and gate of the N-type MOS transistor 2, the source of which is connected to ground voltage V_{SS} (for example, zero volts). A node 15 is connected to the gate of the N-type MOS transistor 3, the drain-source path of which is connected in series between the nodes 14 and 15. The MOS transistors 4a, 4b..., each of which has its gate and source coupled together, are connected in series between the node 15 and the ground voltage V_{SS} , and the MOS transistors 5a,... having their drains and

gates similarly coupled, are connected in series with one another and in parallel with the transistors 4a, 4b...

Operation of the back bias voltage generator of Figure 1 will now be described in more detail.

The square wave output of the oscillator 10 is processed into a square wave which alternates between the level of the source supply voltage V_{CC} and the ground voltage V_{SS} , by means of the buffer circuit 20. The MOS capacitor 1 receives this square wave from the buffer circuit 20 through an output line 12. The input terminal of the MOS capacitor 1 may comprise the source and drain of a MOS transistor coupled together, with the output terminal of the MOS capacitor comprising the gate electrode and being connected to the node 14.

Now, assuming that the square wave delivered to the input terminal of the capacitor 1 is at its rising edge, the voltage V_{CC} charges the capacitor 1 to turn the transistor 2 ON. Then, when the falling edge of the square wave is delivered to the input of the capacitor 1 through the line 12, the voltage at the node 14 on the output side of the capacitor 1 becomes negative and the transistor 2 is turned OFF. At this time, if the voltage of the node 15 connected to the gate of the transistor 3 becomes higher than the negative voltage of the node 14 by an amount at least equal to the threshold voltage of the transistor 3, the transistor 3 turns ON. Thus, the negative charge is transferred from the node 14 to the node 15 through the transistor 3 and the back bias voltage V_{BB} becomes negative. However, if the voltage of the node 14 becomes lower than that of the node 15 by an amount at least equal to the threshold voltage, the transistor 3 turns OFF. Thus the back bias voltage

output at said node 15 returning to an original back bias voltage level, thereby providing a stable back bias voltage output.

5 Referring to Figure 2A, when the source supply voltage V_{cc} suddenly falls to a lower voltage V_{cc}' , as shown by the falling edge 41, the voltage at the node 14 also goes negative and the transistor 3 then turns ON. Thus the back bias voltage at the output node 15 would
10 tend to become further negative, as shown by the negative spike in the waveform 42 of Figure 2B. When the source supply voltage becomes stabilized to the voltage V_{cc} as shown in Figure 2A, the back bias voltage also becomes stabilized to the voltage V_{BB}' as shown in waveform
15 portion 48 of Figure 2B. That is, the back bias voltage becomes more positive by an amount equal to the fall in the source supply voltage, and becomes stable at that level. Then, when the source supply voltage again returns to the voltage level V_{cc} , the back bias voltage
20 would tend to temporarily go up as shown in the spike 44 of Figure 2B, and again come back to the voltage level V_{BB} .

To avoid such spikes, however, the voltage of the
25 node 15 is clamped so that, instead of being of the form shown in Figure 2B, it is of the form shown in Figure 2C. Thus the first negative spike of Figure 2B is clamped as shown by waveform portion 45 of Figure 2C, by means of the series of transistors 4a, 4b,... between the node 15
30 and the ground voltage V_{ss} . If the threshold voltage of each of the transistors 4a, 4b... is V_T and the number of transistors in series connection is K , then the clamping voltage amounts to a value KV_T .

35 Similarly, the transistors 5a,... connected in

series between node 15 and ground voltage V_{SS} are used to prevent the voltage level V_{BB} from increasing beyond a fixed range, as shown in waveform portion 46 of Figure 2C. Thus, although the source supply voltage V_{CC} may vary, the back bias voltage is always clamped to lie within a fixed range.

In a preferred arrangement, the illustrated back bias voltage generator is provided as an on-chip circuit in a semiconductor memory device. As the illustrated back bias voltage generator may prevent reverse breakdown due to negative spike voltage signals such as 42 and forward breakdown due to positive spike voltage signals such as 44 at a junction surface of a semiconductor memory device, stable operation of the semiconductor memory device may be facilitated.

The contents of all papers and documents filed concurrently with this specification are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A semiconductor device including a back bias generator for generating and supplying a back bias
5 voltage to the semiconductor substrate, the generator comprising:

an oscillator for generating a square wave of a predetermined frequency;

10

a buffer connected to receive the square wave output of the oscillator and produce therefrom a similar square wave which alternates between a supply voltage level and another voltage level;

15

a charge pump circuit connected to receive the square wave output of the buffer and produce therefrom a back bias voltage to be applied to the semiconductor substrate; and

20

a clamping circuit which is connected between the output of the charge pump circuit and a ground level and is operative to clamp the level of the back bias voltage so that excursions thereof lie within a predetermined
25 range.

2. A semiconductor device according to Claim 1, wherein said clamping circuit comprises a first set of series connected semiconductor elements arranged to
30 conduct current only in one direction between the output of the pump circuit and said ground level, and a second set of series connected semiconductor elements arranged to conduct current only in an opposite direction between the output of the pump circuit and said ground level,
35 said first and second sets being connected in parallel.

3. A semiconductor device according to Claim 2,
wherein each said semiconductor element comprises an MOS
transistor having a gate electrode connected to a source
or drain electrode thereof.

5

4. A semiconductor device according to any of the
preceding claims, being a semiconductor memory device.

5. A semiconductor device including a back bias
voltage generator which is substantially as hereinbefore
described with reference to the accompanying drawing.

10

15

20

25

30

35